UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,242	12/31/2003	Ryutaro Yamanaka	P24677	6967

7055 7590 10/18/2005

GREENBLUM & BERNSTEIN, P.L.C.
1950 ROLAND CLARKE PLACE
RESTON, VA 20191

EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,242	YAMANAKA ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/5/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Upon further reconsideration, the Examiner hereby withdraws the status of the claims in the previous office action. Claims 1-8 are rejected. This action is non-final.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on August 5, 2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the Examiner. The Examiner would like to point out that most of the NPL was not considered since they were not provided.

Drawings

The drawings are objected to because:

- Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

- Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.
- Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.
- Figure 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed

of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

- Figure 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The specification filed August 5, 2005 is accepted.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially create doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-8 of the present application are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-13 of U.S. Patent No. 6477661. Although the conflicting claims are not identical, they are not patentably distinct from each other. For example, claim 1 of the present application teaches a digital signal processor capable of performing a Viterbi algorithm comprising: an instruction fetching unit that fetches instructions; a decoding unit that decodes the instructions fetched by the instruction fetching unit; and an execution unit that executes the instructions decoded by the decoding unit, the execution unit comprising: an arithmetic logic unit configured to perform a register-register arithmetic logic operation, wherein the arithmetic logic unit compares a first data with a second data, in parallel with a comparison of a third data with a fourth data, and the execution unit outputs new path metrics; and wherein the first data, the second data, the third data, and the fourth data can each be one of four results obtained by adding one of two path metrics to one of two branch metrics. Whereas claim 4 of the Reference '661 teaches a digital signal processor capable of performing a Viterbi algorithm comprising: an instruction fetching system that fetches instructions; a decoding system that decodes the instructions fetched by the instruction fetching

system; and an executing system that executes the instructions decoded by the decoding system, the executing system comprising: a first comparing system that compares a first data that includes a sum of a path metric PM1 of an old state 2N and a branch metric BM1 with a second data that includes a sum of a path metric PM0 of an old state 2N+1 and a branch metric BM0; and a second comparing system that compares a third data that includes a sum of the path metric PM 1 and branch metric BM0 with a fourth data that includes a sum of the path metric PM0 and the branch metric BM1, where N=0, 1, . . . , 2.sup.K-2 -1, and where K represents a constraint length, wherein the first comparing system and the second comparing system operate together. The remaining limitations of claim 1 of the present application are taught in claim 7 of the Reference '661. The combination of claims 4 and 7 of the reference '661 teach the claim 1 of the present application. Therefore claim 1 of the present application is an obvious embodiment of claim 4 of the reference '661. The examiner would like to point out that similar reasoning applies to independent claim 4 of the present application as well.

Again the examiner would like emphasize that although the two inventions are not 'exactly' the same, they are **not patentably distinct** because the process remains the same and hence one is just an embodiment of the other.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2 and 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is "any two" is referring to in the claim.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Araki et al. (USPN 5946361) further in view of Yamashita et al. (USPN 4614933).

As per claims 1 and 3, Araki et al. (herein after referred to as one entity: Araki) substantially teaches a Viterbi decoding circuit that stores comparison result bits in a bit-accessible path memory unit. A back-trace is performed by setting a state value in a shift register, then shifting comparison result bits from the path memory unit into the shift register. A certain number of bits at the shift-in end of this register are supplied as read address bits to the path memory unit. In a second aspect, a Viterbi decoding circuit has selectors that first select old path metric values and branch metric values, which are added or subtracted to produce candidate path metric values, then select the candidate path metric values, which are subtracted to produce a comparison result bit representing the sign of their difference. These additions and

subtractions are performed by the same arithmetic unit. Araki teaches that some of the operations that have been described as being carried out by hardware can also be performed by software. The decrement operation carried out by the address incrementer 13 in FIG. 5, for example, can be performed by an instruction unit that decrements a register (used as the address register 11) in the processor 1. The conventional arithmetic and logic unit in the processor 1 can also be employed as the address adder 15, so that the entire address generating unit 7 is implemented using existing processor facilities.

Araki does not explicitly teach a ALU to compare a first data with a second data in parallel with a comparison of a third data with a fourth data to determine new path metrics as stated in the present application.

However, Yamashita et al. (herein after referred to as one entity: Yamashita) teaches, in an analogous art, a Viterbi decoder with a pipeline processing function for decoding a received code sequence transferred from an encoder, including correlation determining circuit for calculating correlation between a received code sequence and each of a plurality of predetermined code sequences of known allowable transitions; and selecting circuits operatively receiving the correlations for selecting one of the predetermined code sequences as the maximum likelihood transition. The selected one of the predetermined code sequences has the maximum correlation among the correlations. A decoded code sequence is obtained from the selected one of the predetermined code sequences. The correlation determining circuit includes a plurality of new correlation determining circuits each for determining a new correlation based on newly received code sequence and an already calculated correlation between the already received code sequence and one of the predetermined code sequences; and a comparing circuit for comparing,

simultaneously with the determination of the new correlations, already calculated correlations between the already received code sequence and the predetermined code sequences, so as to output a path selecting data. The selecting circuits selects, in response to the selecting data, one of the predetermined code sequences as the maximum likekihood sequence with respect to the code sequence generated by the encoder. Particularly, Yamashita teaches (Figure 7) to compare a first data with a second data in parallel with a comparison of a third data with a fourth data to determine new path metrics.

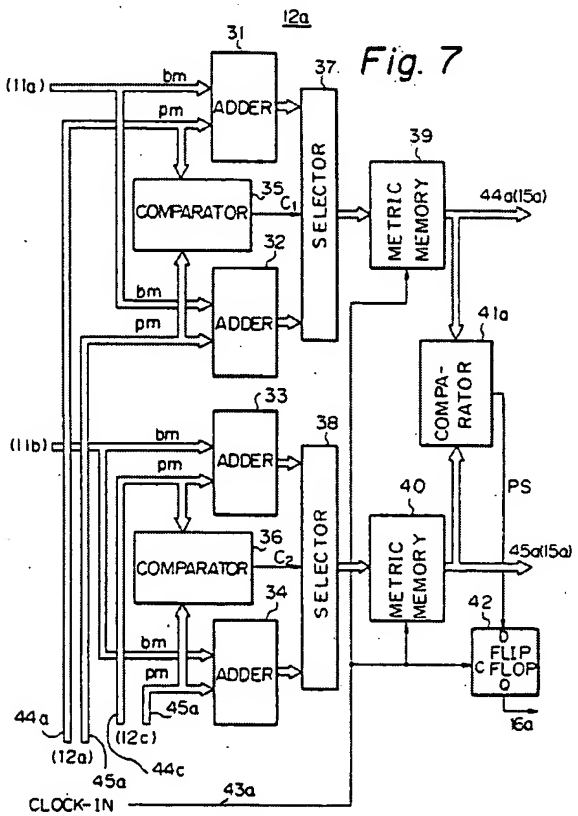

Fig. 7

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to compare a first data with a second data in parallel with a comparison of a third data

with a fourth data to determine new path metrics. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by comparing a first data with a second data in parallel with a comparison of a third data with a fourth data to determine new path metrics would have decreased the power consumption and thus improved the Viterbi decoding process.

As per claim 2, Yamashita substantially teaches, in view of above rejections, (Figure 7) to output new path metrics through metric memories 39 and 40.

As per claims 4 and 6, Araki et al. (herein after referred to as one entity: Araki) substantially teaches a Viterbi decoding circuit that stores comparison result bits in a bit-accessible path memory unit. A back-trace is performed by setting a state value in a shift register, then shifting comparison result bits from the path memory unit into the shift register. A certain number of bits at the shift-in end of this register are supplied as read address bits to the path memory unit. In a second aspect, a Viterbi decoding circuit has selectors that first select old path metric values and branch metric values, which are added or subtracted to produce candidate path metric values, then select the candidate path metric values, which are subtracted to produce a comparison result bit representing the sign of their difference. These additions and subtractions are performed by the same arithmetic unit. Araki teaches that some of the operations that have been described as being carried out by hardware can also be performed by software. The decrement operation carried out by the address incrementer 13 in FIG. 5, for example, can be performed by an instruction unit that decrements a register (used as the address register 11) in the processor 1. The conventional arithmetic and logic unit in the processor 1 can also be

employed as the address adder 15, so that the entire address generating unit 7 is implemented using existing processor facilities.

Araki does not explicitly teach a ALU to compare a first data with a second data in parallel with a comparison of a third data with a fourth data to determine new path metrics as stated in the present application.

However, Yamashita et al. (herein after referred to as one entity: Yamashita) teaches, in an analogous art, a Viterbi decoder with a pipeline processing function for decoding a received code sequence transferred from an encoder, including correlation determining circuit for calculating correlation between a received code sequence and each of a plurality of predetermined code sequences of known allowable transitions; and selecting circuits operatively receiving the correlations for selecting one of the predetermined code sequences as the maximum likelihood transition. The selected one of the predetermined code sequences has the maximum correlation among the correlations. A decoded code sequence is obtained from the selected one of the predetermined code sequences. The correlation determining circuit includes a plurality of new correlation determining circuits each for determining a new correlation based on newly received code sequence and an already calculated correlation between the already received code sequence and one of the predetermined code sequences; and a comparing circuit for comparing, simultaneously with the determination of the new correlations, already calculated correlations between the already received code sequence and the predetermined code sequences, so as to output a path selecting data. The selecting circuits selects, in response to the selecting data, one of the predetermined code sequences as the maximum likekihood sequence with respect to the code sequence generated by the encoder. Particularly, Yamashita teaches (Figure 7) to compare a

first data with a second data in parallel with a comparison of a third data with a fourth data to determine new path metrics. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to compare a first data with a second data in parallel with a comparison of a third data with a fourth data to determine new path metrics. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by comparing a first data with a second data in parallel with a comparison of a third data with a fourth data to determine new path metrics would have decreased the power consumption and thus improved the Viterbi decoding process.

As per claim 5, Yamashita substantially teaches, in view of above rejections, (Figure 7) to output new path metrics through metric memories 39 and 40.

As per claims 7 and 8, Araki substantially teaches, in view of above rejections, (col. 1) convolutional codes are employed in mobile communication systems ranging from cellular telephone networks to earth satellite systems. A convolutional coder generates output bits from the k most recent input bits, where k is an integer referred to as the constraint length. The most recent k-1 of these bits identify what is called a state, with input of each new bit causing a transition to a new state. At any given time there are 2.sup.k-1 possible states. The Examiner would like to point out that it is well known in the art for Viterbi decoding to be performed in mobile and base stations.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts are included herein for Applicant's review.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mujtaba Chaudry
Art Unit 2133
October 6, 2005

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100